From September 2005 High Frequency Electronics

Reference-Clock Generation for Sampled Data Systems

By Paul Nunn
Dallas Semiconductor Corp.

The performance of the reference clock establishes the overall timing accuracy and phase noise performance in today's digital communications using wireless, wireline and optical transmission

This article examines the characteristics and performance of a reference clock for a sampled-data system. Reference clocks with excellent performance are required in GSM and UMTS wireless base stations and in telecom-system subsections such as routers, add-drop multiplexers, and aggregation boxes. The reference clock in those systems is generally derived from a crystal-based module such as an XO, TCXO, VCXO, or OCXO. In turn, those devices are usually chosen to obtain the required frequency stability, jitter and phase noise performance. Within the last four years these modules have come to offer much smaller dimensions, higher fundamental crystal frequencies, improved phase noise and reduced jitter—all with substantial price reductions.

Poor phase noise performance and excessive jitter from a reference clock can easily cause a large degradation of SNR in the signal path. Without understanding the need to specify proper reference clock characteristics, a systems designer can spend lots of time debugging the system timing and other data-related phenomena associated with development efforts. Over-specifying clock performance can cause higher costs in a custom development.

The generation of stable and coherent frequencies for carrier and clock is a necessity for the sampled-data systems of high-speed digital communications. For that purpose, this article examines the properties and statistical description of phase noise on signals produced by the primary and secondary oscillators used in generating such reference signals.

To design and characterize the behavior of systems that generate coherent reference signals, you must statistically describe an oscillator's phase noise. The reference signal can be modeled with the following equation:

$$r(t) = A\left[1 + a(t)\right]\cos\left[\omega_s t + \varphi(t) + \frac{\alpha t^2}{2}\right] \qquad (1)$$

where $\omega_s = 2\pi f_s$ is the nominal reference frequency of interest, $\varphi(t)$ is random phase jitter, and the term $\alpha t^2/2$ describes the phase accumulation due to long-term frequency drift in the oscillator [1].

Phase jitter, $\varphi(t)$, can occur at the output of a primary reference source such as a transmitter synthesizer block. It can also accumulate in a system that links several system oscillators in a network. Phase jitter can include the effects of component aging, fluctuations in temperature and supply voltage, and even random noise.

Reference oscillators are critical for accurate timing in high-frequency digital communication systems, because they drive high-performance analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and digital signal processors (DSPs). Excessive phase noise (jitter) in the reference oscillator will affect the whole system. Thus, selecting a good reference oscillator allows calculation of a tolerable jitter budget in the rest of the system and eliminates many of the jitter-related issues associated with debugging the system.

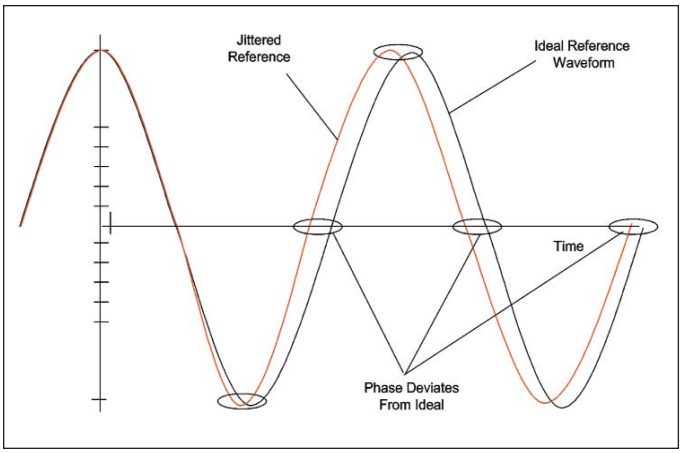

Figure 1 · Jitter effects on a sinusoidal reference.

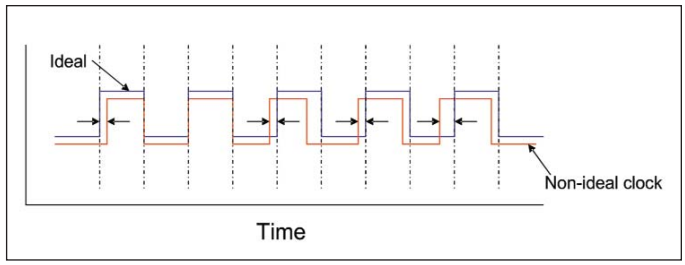

Figure 2 · Jitter effects on a square-wave reference.

Foundation

Digital communication systems employ ADCs and DACs to manipulate analog signals for transmission and reception. Conversion processes add error, and (more importantly) they degrade the original voice, video or other analog information. The goal, therefore, is to recover the original signal without loss of the critical characteristics necessary in discerning the intent of the original message.

DACs routinely operate at conversion rates greater than 1 GHz in today's high-performance systems, and ADCs operate at conversion speeds exceeding 250 MHz, with resolutions as high as 16 bits. Stability, phase noise and jitter in the reference oscillator directly affect the performance of these systems.

In applications that involve wireless infrastructure equipment, a converter with high spurious-free dynamic range (SFDR) can capture weak signals in the frequency band of interest despite the presence of interfering signals. SFDR is the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component. (The peak spurious component may or may not be a harmonic [5].)

High-speed ADC systems are extremely sensitive to the quality of the sampling clock. Because the operation of a track-and-hold circuit is similar to that of a mixer, any noise, distortion, or timing jitter on the clock combines with the desired signal at the ADC output to degrade the sampled signal. The degradation of an ADC's SNR at a given input frequency can be calculated if the RMS amplitude due only to aperture jitter (tj) is known:

$$\mathrm{SNR} = 20\log\left[2\pi f_{IN} * tj\right] \tag{2}$$

Aperture jitter (tj), the root-mean-square of all jitter sources including that of the sampling clock, is defined as the sample-to-sample variation between the rising of the sampling clock and the instant the analog signal is sampled. For an ideal data converter, the worst-case signal-to-noise ratio is provided by the following equation [3, 4]:

$$\mathrm{SNR}_{\mathrm{IDEAL}} = 6.02(N) + 1.76 \tag{3}$$

where N is the converter's resolution in bits [1].

Reference-Oscillator Noise Characteristics

In reviewing the reference-clock model described by equation (1), we can, by simplifying the expression, provide boundaries for examining the behavior of the jitter component $\varphi(t)$. First, we assume the function $a(t)$ negligibly affects amplitude modulation on the reference-clock model. (The effect of the phase accumulation term $\alpha t^2/2$ on the sample clock $r(t)$ is beyond the scope of this article.) Removal of these terms reduces the model to the following equation [1]:

$$r(t) = A\cos\left[\omega_s t + \varphi(t)\right] \tag{4}$$

Many treatments of this model explore the statistical properties of $\varphi(t)$, including its standard deviation or variance and even its power spectral density. For example, "Assuming that $\varphi(t)$ has zero mean, its variance can be obtained by integrating the phase-jitter power spectral density, $G_\varphi(f)$, with units of rad^2/Hz over all frequency." [1] From that relation, the power spectral density of instantaneous frequency fluctuation can be related to the phase-jitter power spectral density by $S_\omega(f) = (2\pi f)^2 G_\varphi(f)$ (rad/s)^2/Hz.

To place boundaries on the effect of $\varphi(t)$ in a sampled-data system, we can graphically evaluate the effects of jitter on the cosine or sine function. Figure 1 shows that phase jitter creates a deviation from the ideal cosine waveform at the zero-crossing points. The same effect can be demonstrated for a square-wave reference (Figure 2). Such deviations can be defined or quantified using the various definitions of jitter: cycle-to-cycle jitter, RMS jitter, or peak-to-peak jitter. The peak-to-peak variations shown in Figure 2 provide an illustration of how widely the phase variations can deviate from the ideal case. For sampled-data systems, these variations

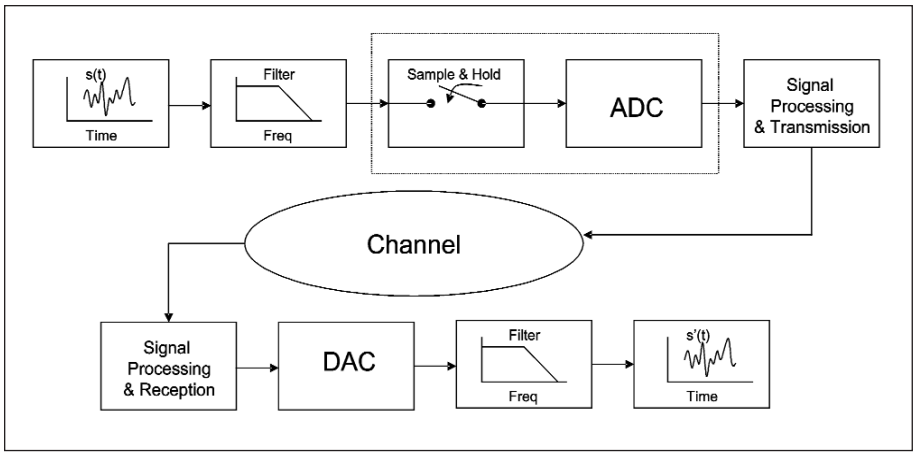

Figure 3 · Frequency spectrum of an arbitrary signal *s(t)*.

degrade overall performance as indicated by the system signal-to-noise ratio (SNR), total harmonic distortion (THD) and SPDR.

Ideal Sampling and Conversion

To begin an evaluation of the effect of clock jitter on an ADC, we first examine the ADC's sampling frequency (f_s) and its number of quantization levels (2^N–1). The sampling frequency (which appears in equation 1) is used in Nyquist's Theorem to reconstruct an analog signal from sampled data. A typical sampled data system is shown in Figure 3.

The number of quantization levels 2^N–1 is also the total number of discrete levels available for representing the sampled analog signal. An N-bit DAC or ADC therefore allows 2^N–1 different quantization levels. For an ideal data converter, the worst case signal-to-noise ratio (SNR) is calculated using equation (3), where N is the converter's number of bits. Thus, for a 10-bit DAC, the ideal SNR is 61.96 dB.

To understand how a sampling clock's jitter can affect the performance of an ADC or DAC, we use the arbitrary signal $s(t)$ shown in Figure 4 to evaluate what happens when a signal is sampled. We assume that $s(t)$, if not periodic, is bounded over a specified time interval $[t_0, t_0+T]$.

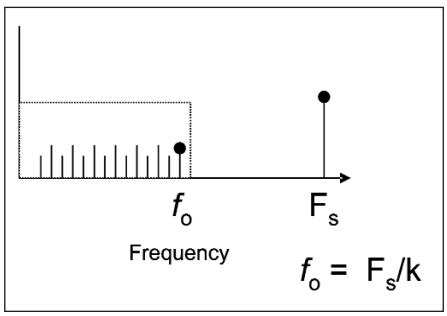

Figure 4 · A typical sampled-data system.

Figure 3 shows the individual frequency components that compose $s(t)$. Nyquist's Theorem states that a sampling clock must have a frequency value (F_s) at least twice as great as the highest frequency content of the signal of interest. Note for the frequency spectrum of $s(t)$ (Figure 3, within the box), the highest frequency content is f_0. The relationship $f_0 = F_s/k$, where $k = 2$, shows the necessary relationship between sampling clock and signal of interest to prevent inter-symbol interference, as prescribed by Nyquist. (Inter-symbol interference occurs for $k < 2$.) If $s(t)$ is bounded by f_0, the greatest rate of change in $s(t)$ is attributable to the frequency f_0.

We assume the magnitude of the f_0 contributor is on the order of all other frequency contributors to $s(t)$, and is not negligible with respect to

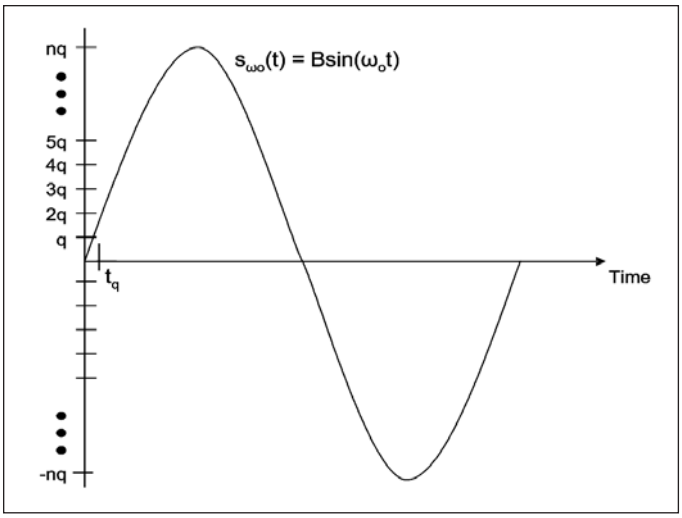

Figure 5 · Time-domain representation of $s_{\omega 0}(t)$.

the ADC's smallest quantization step. Given these assumptions, and for the purpose of simplification, let $s_{\omega 0}(t)$ be represented by the following equation:

$$s_{\omega o}(t) = B\sin(\omega_0 t) \tag{5}$$

where B is the amplitude of $s_{\omega 0}(t)$ and $\omega_0 = 2\pi f_0$. Let the amplitude [B] of $s_{\omega 0}(t)$ equal the full range of the ADC. A time-domain representation of $s_{\omega 0}(t)$ (Figure 5) includes the quantization levels.

Next, examine $s_{\omega 0}(t)$ to determine where the greatest rate of change occurs. Applying the first derivative to $s_{\omega 0}(t)$ and plotting that function over the time interval shown for $s_{\omega 0}(t)$ confirms that the greatest rate of change occurs as the amplitude of $s_{\omega 0}(t)$ approaches zero. Our interest in this area of the curve is important, both for jitter considerations and for the impact of jitter on the sampling performance of the ADC (or DAC). If the jitter exceeds a certain time boundary, the ADC's sampling or decision point may be in error for critical areas of the curve. That behavior effectively reduces the ADC's bit resolution and can be equated back to the ideal SNR for an N-bit ADC or DAC.

For this example we define $q = B/[2^N–1]$, where q equals the step size for a single quantized level of the ADC, and N is the number of bits for the ADC or DAC. Using $s_{\omega 0}(t)$, we seek to define a time value (t_q) that provides a boundary on reference clock jitter. If reference clock jitter exceeds the value of t_q, you can then determine by how much the degradation (with respect to the ADC's ideal SNR) is affected by the reference clock.

We begin by making the following relation between t_q and q in equation (6),

$$s_{\omega o}(t_q) = q = B\sin(2\pi f_o t_q) \tag{6}$$

and then relating this equation back to the number of bits in the ADC:

$$\frac{q}{B} = \sin(2\pi f_o \cdot t_q) \tag{7}$$

$$\frac{q}{B} = \frac{1}{[2^N - 1]} \tag{8}$$

Substituting equation (8) into equation (7),

$$\frac{1}{(2^N - 1)} = \sin(2\pi f_o \cdot t_q) \tag{9}$$

and solving for t_q,

$$2\pi f_o \cdot t_q = \sin^{-1}\left(\frac{1}{[2^N - 1]}\right) \tag{10}$$

$$t_q = \sin^{-1}\frac{\left(\frac{1}{[2^N - 1]}\right)}{(2\pi f_o)} \tag{11}$$

it can be shown that for N >>1:

$$\sin^{-1}(1/[2^N–1]) \cong 1/[2^N–1]$$

Using that approximation, you can write t_q as

$$t_q = \frac{\left(\frac{1}{[2^N - 1]}\right)}{(2\pi f_o)} \tag{12}$$

You can use a t_q value at this stage to provide a boundary for acceptable levels of jitter. If the jitter of the reference clock exceeds that of t_q, you can surmise that the SNR of the ADC or DAC will be degraded. If you wish to see the effect of jitter for values of $t > t_q$, solve for N in equation (12) to provide an outlook on the effective number of bits (ENOB) of an ADC or DAC for the given time $t > t_q$:

$$N = \log_2\left[\frac{1}{(2\pi f_o \cdot t)} + 1\right]. \ (t \geq t_q) \tag{13}$$

By substituting for N in equation (3), $(6.02N + 1.76)$ you can estimate by how much the jitter will degrade the

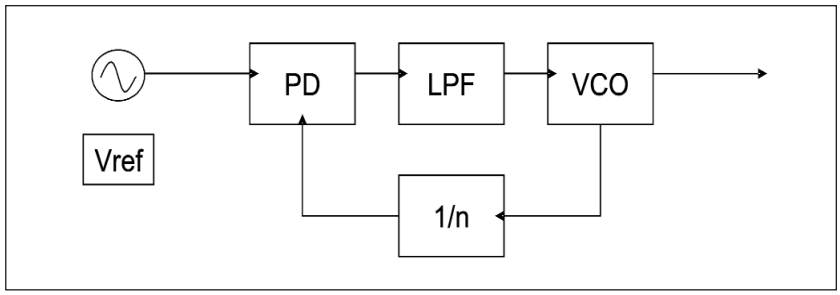

Figure 6 · General block diagram for a PLL.

SNR from the ideal case based on the time $t > t_q$.

For practical considerations, the value of t_q cannot be assigned to the reference clock alone. If we consider the definition of aperture jitter and its effect on ADC performance, the reference clock may have to perform much better than t_q. As defined earlier, aperture jitter is the sample-to-sample variation in the time intervals between the rising of the sampling clock and the instant the analog signal is sampled.

The Reference Oscillator and the PLL

For applications in which frequency multiplication is required (generating a reference greater than 100 MHz, for example), the primary choice is a PLL. Again, the primary source for driving the PLL (Figure 6) is a crystal-based reference oscillator. The PLL-based reference generally consists of five sections, which include a crystal-based oscillator as the reference, a phase detector, a voltage-controlled oscillator (VCO), dividers and loop filters.

The crystal-based reference is generally chosen for its stability over temperature as well for the desired noise performance. Any noise generated in the crystal-based reference will be multiplied by a factor n inside the PLL loop, where n is the desired multiplication factor. If equation (4) is the model used for the crystal-based reference, then the output of a PLL (or frequency multiplier) can be represented as follows:

$$m(t) = P\cos\left[n\omega_c t + n\varphi(t)\right] \quad (14)$$

where n is the multiplication factor and ω_c is the center frequency of the VCO.

Noise generation in the PLL loop comes from the phase detector and the VCO, as well as the charge-pump circuits. Multiplication of the reference oscillator input can be seen in a phase-noise plot of the PLL output. The loop acts as a bandpass filter over the loop bandwidth of the phase detector (charge pump).

Summary

This article examines certain characteristics necessary in the understanding and modeling of reference-oscillator jitter, as applied to wireless and digital communication systems using ADCs and DACs. The performance of reference oscillators is critical to the timing of today's high frequency digital communication systems. As shown, excess jitter (phase noise) at the reference-oscillator level can impact the overall system, including any multiplication of the reference signal. Understanding and planning for the jitter sources in a system aids in developing a practical jitter budget, and in selecting components based on the specifications for those sources.

References

1. Rodger E. Ziemer and Rodger L. Peterson, *Digital Communications and Spread Spectrum Systems*, Macmillan 1985.

2. Leon W. Couch II, *Digital and Analog Communication Systems*, 1983, Macmillan.

3. Bar-Giora Goldberg, "The Effects of Clock Jitter on Data Conversion Devices," *RF Design*, August 2002.

4. Bonnie Baker, "What does the ADC SNR Mean?," *EDN*, May 27, 2004.

5. Application Note AN-282, "Fundamentals of Sampled-Data Systems," Analog Devices.

Author Information

Paul Nunn is Business Manager, Precision Oscillators at Dallas Semiconductor Corp. (part of Maxim Integrated Products, Inc.) He can be reached by e-mail at: Paul.Nunn@dalsemi.com.

Writing for *High Frequency Electronics*

We have very simple guidelines for authors wishing to submit an article for publication in *High Frequency Electronics*:

1. Prepare a description of the article—this can be an abstract, outline, informal description, a draft manuscript or even the finished piece.

2. Send the above description to Editorial Director Gary Breed—by e-mail to gary@highfrequency-electronics.com or by post or shipping company to: High Frequency Electronics, 403 Venture Ct. #7, Verona, WI 53593.

We will review the proposed article and follow up with an expected publishing schedule, suggestions for improvement, or other feedback.

Topics of Interest in 2006

A few of the subject areas we will cover next year include: standards and regulations, military applications, high speed digital techniques, sensors, wide bandwidth technologies, mm-wave technology, high power design, HF (<50 MHz) applications, engineering education, passive components, optical technologies, wafer-scale measurements, digital signal processing—plus nearly any other topic of interest to our engineering readers.